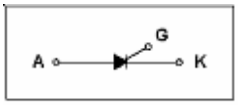
Shantou Huashan Electronic Devices Co.,Ltd.

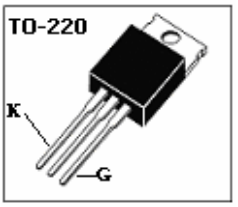
HBT151

Silicon Controlled Rectifier

Features

*** Repetitive Peak Off-State Voltage : 600V**
*** R.M.S On-State Current($I_{T(RMS)}$=12A)**
*** Average On-State Current ($I_{T(AV)}$=7.5A)**
*** Non-isolated Type**





General Description

Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

Absolute Maximum Ratings (T_a=25℃ unless otherwise specified)

T_{stg}——Storage Temperature ---------- -40~150℃
T_j ——Operating Junction Temperature ---------- 125℃
V_{DRM} ——Repetitive Peak Off-State Voltage ---------- 600V
I_T (RMS) ——R.M.S On-State Current (all conduction angles) ----------12A
$I_{T(AV)}$ ——Average On-State Current (Half Sine Wave : T_C = 109 °C) ----------7.5A
I_{TSM} ——Surge On-State Current (1/2 Cycle, 50Hz, Sine Wave, Non-repetitive) ---------- 100A
I^2t ——Circuit Fusing Considerations(t = 10ms) ---------- $50A^2s$
P_{GM} ——Forward Peak Gate Power Dissipation (T_a=25℃) ---------- 5W
$P_{G(AV)}$ ——Forward Average Gate Power Dissipation (over any 20 ms period) ----------0.5W
I_{FGM} ——Forward Peak Gate Current ---------- 2A
V_{RGM} ——Reverse Peak Gate Voltage ---------- 5V

Electrical Characteristics (T_a=25℃ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
I_{DRM}	Repetitive Peak Off-State Current			20 500	uA	$V_{AK}=V_{DRM}$ T_c=25℃ T_c=125℃
V_{TM}	Peak On-State Voltage (1)			1.75	V	I_{TM}=23A,tp=380μs
I_{GT}	Gate Trigger Current (2)			15	mA	V_{AK} =12V(DC), R_L=10 ohm
V_{GT}	Gate Trigger Voltage (2)			1.5	V	V_{AK} =12V(DC), R_L=10 ohm T_c=25℃
V_{GD}	Non-Trigger Gate Voltage	0.2			V	V_{AK} =12V, R_L=100 ohm T_c=125℃
I_H	Holding Current			20	mA	I_T=100mA,Gate open, T_c=25℃
Rth(j-c)	Thermal Resistance			1.3	℃/W	Junction to Case
Rth(j-a)	Thermal Resistance		60		℃/W	Junction to Ambient
dv/dt	Critical Rate of Rise Off-state Voltage	50			V/μs	Linear slope up to V_D=V_{DRM}67% Gate open Tj=125℃

1. Forward current applied for 1 ms maximum duration,duty cycle ≤1%.
2. R_{GK} current is not included in measurement

Performance Curves

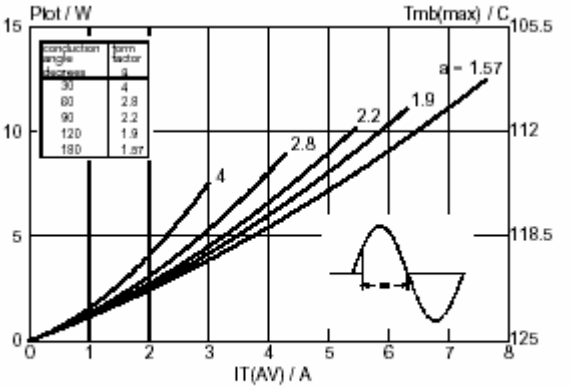


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$

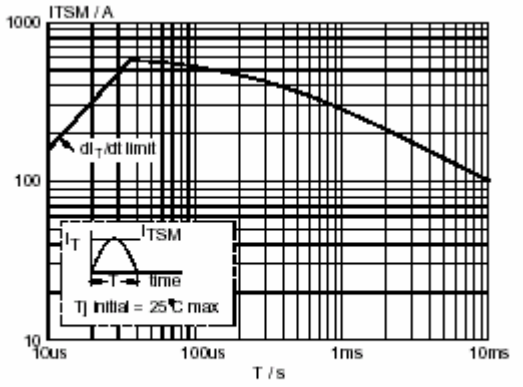


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, t_p ≤ 10ms.

Performance Curves

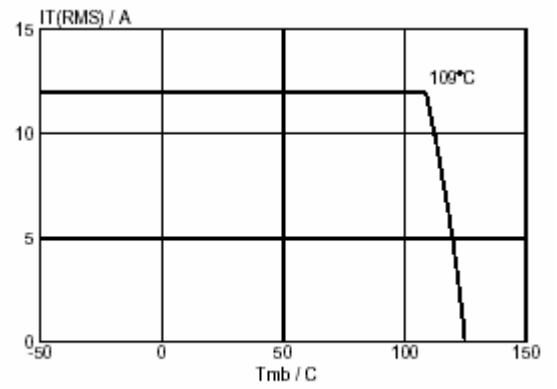


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

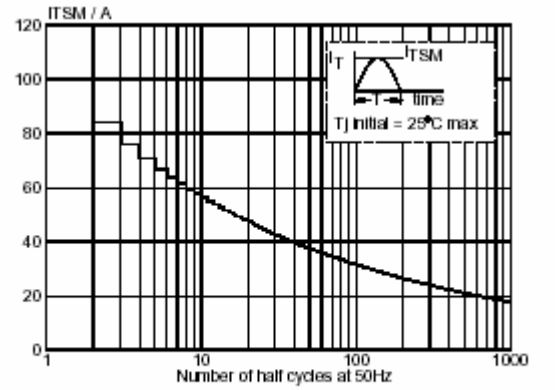


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

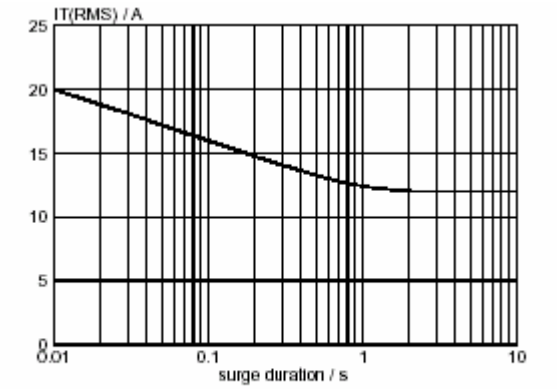


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 109$˚C.

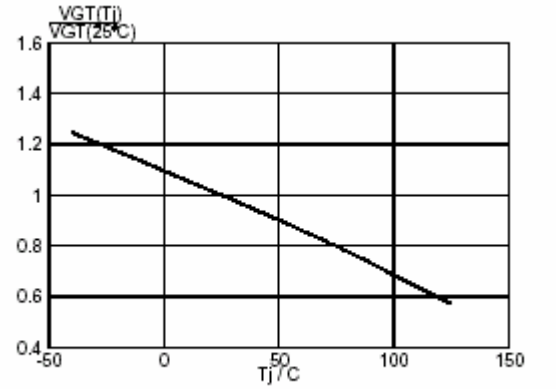


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature T_j.

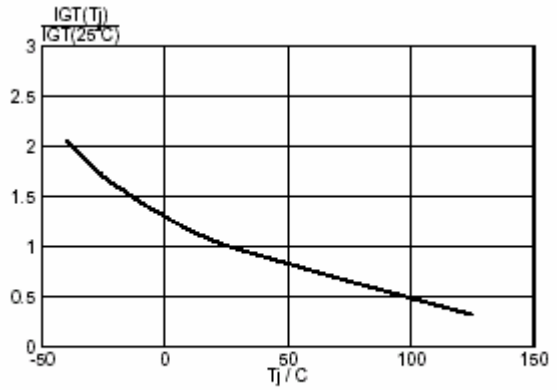


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

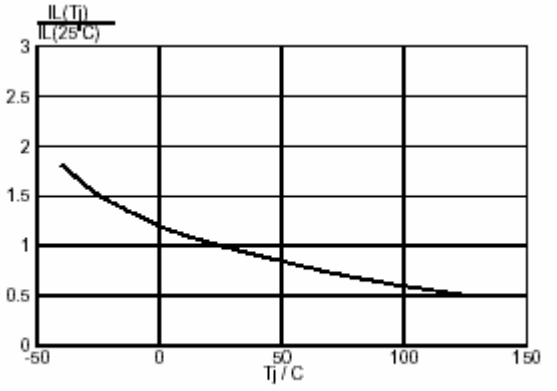


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

Performance Curves

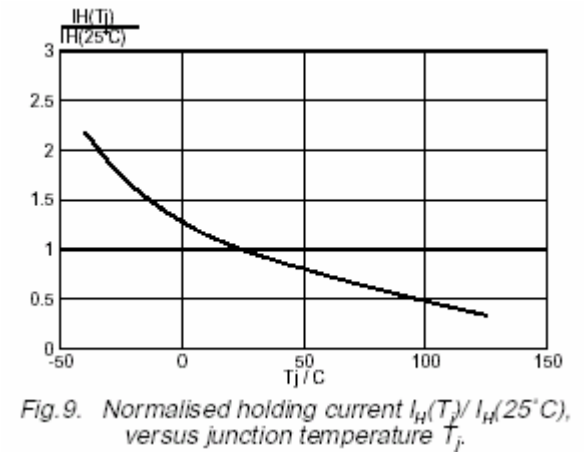


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^\circ C)$, versus junction temperature T_j.

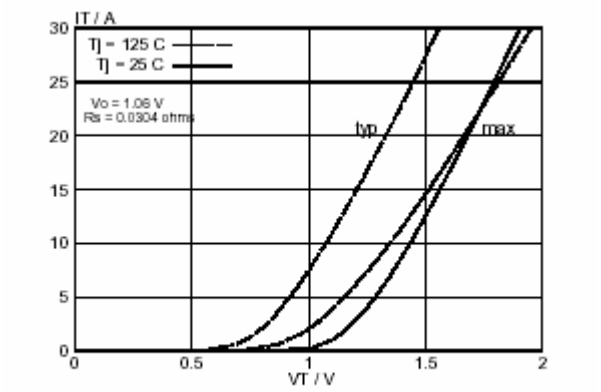


Fig.10. Typical and maximum on-state characteristic.

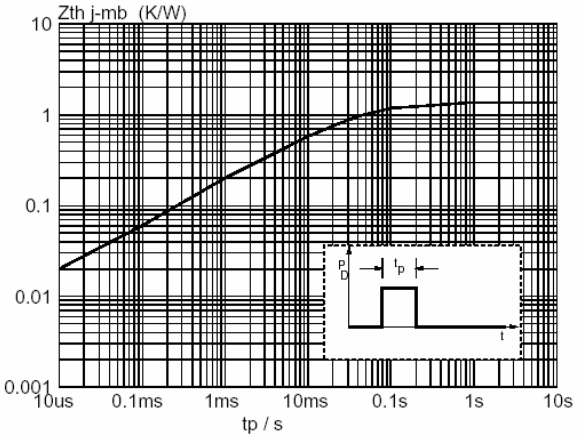


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

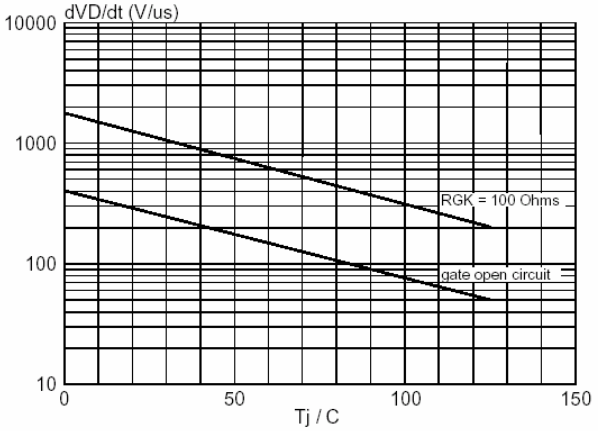


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.